

METHODS FOR FORMING ISOLATION TRENCHES INCLUDING DOPED SILICON OXIDE

FIELD OF THE INVENTION

The present invention relates to the field of microelectronics and more particularly to isolation methods for microelectronic devices.

BACKGROUND OF THE INVENTION

The formation of an isolation trench can be an initial step in the fabrication of a microelectronic device. As such, the formation of the isolation trench influences the size of the active areas and processing margins for the following steps in the fabrication process. In the past, the local oxidation (LOCOS) method has been widely used to form isolation layers. As microelectronic structures have become more highly integrated and the width of the isolation layers has decreased, the bird's beak phenomenon has adversely affected the performance characteristics of the resulting devices. In addition, the thermal processing of the LOCOS method may cause defects in the crystal structure of the substrate, as well as distribution of dopants implanted therein. These effects may further degrade the operational characteristics of the microelectronic devices formed by the LOCOS method.

The trench isolation method has been developed to provide relatively small isolation areas on a microelectronic substrate. According to this method, a trench is formed in the substrate, and this trench is filled with an insulating material. The thickness of the isolation layer can thus be increased. Furthermore, the isolation can be formed by methods other than thermal oxidation so that defects caused by the thermal oxidation step of the LOCOS method can be reduced.

When forming a microelectronic device using the trench isolation method, however, it may be difficult to completely fill the trench with the insulating material without forming a void in the insulating material. In particular, when filling a trench with an insulating oxide layer using chemical vapor deposition (CVD) techniques, a void may be formed in the trench if the oxide does not have complete conformity. This void may later be exposed during a subsequent etch step, and a portion of the material used to form a gate electrode may remain in this void after patterning the gate electrode. This material may cause a short circuit between conductive layers thus reducing the yield and reliability of microelectronic devices formed thereby.

A conventional method for reducing the void when filling the trench will now be described with reference to FIGS. 1A-1D. As shown in FIG. 1A, a trench can be formed by etching an isolation region of the substrate 2 to a predetermined depth. An oxide layer 4 can be formed on the surface of the etched substrate to reduce stress between the substrate and the trench filling material which can be a polysilicon layer 6. The polysilicon layer 6 can be used as a mask to protect the substrate during a subsequent etch step which planarizes the surface of the material used to fill the trench. A nitride layer 8 can serve as a barrier layer to prevent doping of the substrate.

A doped oxide layer 10 having a thickness of 2.5 μm can be deposited on the nitride layer 8 as shown in FIG. 1B. In particular, the doped oxide layer 10 can be formed by chemical vapor deposition (CVD). Because the deposition rate of the CVD doped oxide layer 10 is faster at the upper corners of the trench than at the bottom or sidewalls of the trench, the void 12 may form in the trench. By heating the

doped oxide layer 10 to a temperature in the range of 950° C. to 1,150° C. for about 30 minutes, the doped oxide layer 10 may reflow as shown in FIG. 1C. The void 12 is thus filled, the thickness of the oxide layer 10 is lowered, and the surface of the oxide layer is planarized.

As shown in FIG. 1D, the doped oxide layer 10, the nitride layer 8, and the polysilicon layer 6 can be etched back until the surface of the oxide layer 4 is exposed. The oxide layer 4 can then be selectively removed to expose active regions of the substrate 2. As shown, the trenches are filled with the remaining portions of the doped oxide layer 10, the nitride layer 8, the polysilicon layer 6, and the nitride layer 4. According to this method, the doped oxide layer can be provided by a boro-silicate glass (BSG), a phospho-silicate glass (PSG), or a borophosphorous-silicate glass (BPSG), and each of these materials can be deposited by chemical vapor deposition. Furthermore, these doped oxides can be reflowed at high temperatures to fill the void.

The doped oxide, however, may have a faster etching rate than a thermal oxide as shown in the graph of FIG. 2. In particular, FIG. 2 shows the etch rate of a borophosphorous-silicate glass in circles, and the etching rate of the thermal oxide is shown with rectangles. The relative etching rates of various oxides is discussed, for example, at page 217 of "Silicon Processing For The VLSI Era" by S. Wolf. Accordingly, a doped oxide layer filling the trench may be excessively etched during subsequent processing steps such as removing a pad oxide layer, removing a sacrificial oxide layer, and removing an ion implant buffer layer. As a result, the oxide layer remaining in the trench may not reach the surface of the substrate. Because portions of the trench sidewalls may be exposed, the gate of an adjacent transistor may cover the upper edge of the trench thereby causing a greater electric field at the edge of the trench than at the center of the channel. A hump phenomenon may thus occur causing a transistor to turn on twice as illustrated in FIG. 3. This hump phenomenon may reduce the performance characteristics of the transistor.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide improved methods for forming isolation trench structures.

It is another object of the present invention to provide methods for reducing voids in isolation trench structures.

It is still another object of the present invention to provide methods which increase an etch resistivity of an oxide layer for an isolation trench structure.

These and other objects are provided according to the present invention by methods including the steps of forming a trench in a substrate, forming an insulation layer which fills the trench, implanting ions into the insulating layer which decrease an etch rate of the layer, and removing portions of the insulating layer on the substrate while maintaining the insulating layer in the trench. By implanting ions which decrease the etch rate of the insulating layer, the isolation trench structure can be formed without significantly exposing the sidewalls of the trench. In particular, mask layers used to form the trench and left on the substrate when forming the insulating layer can be selectively removed without overetching the insulating layer in the trench or significantly exposing sidewalls on the trench.

In particular, the implanting step may include implanting nitrogen (N^+) ions at a dose on the order of 1×10^{13} to 1×10^{18} ions/cm². This dose of nitrogen is sufficient to increase the etch resistivity of the oxide layer to thus decrease the etching rate. The step of forming the insulating layer may include